

AMENDMENT

Amendment to the claims

Listing of claims:

Claim 3, 4, 5 and 8 were cancelled.

Claim 1 (currently amended): A method of processing signals of a timing controller of a liquid crystal display module, comprising the steps of:

- (a) receiving a vertical synchronizing signal;
 - (b) receiving a data enable signal DE which has a vertical blank period;
 - (c) generating a gate clock signal CPV which has a plurality of gate clock cycles C1-Cn;
 - (d) after a rising edge or a falling edge of the vertical synchronizing signal, generating a plurality of gate-on enable signals OE simultaneously according to the plurality of gate clock cycles C1-Cn of the gate clock signal CPV; [and]
 - (e) after a rising edge or a falling edge of the vertical synchronizing signal, generating start vertical signals STV before the end of the vertical blank period VB and after at least a gate clock cycle C1 during the vertical blank period VB, wherein the start vertical signals STV includes a first start vertical signal STV1 to determine a start scan location of a frame and a second start vertical signal STV2 to offset flicker and display brightness of the liquid crystal display; and
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- (f) pausing output of CPV, STV₁, and OE until the end of the vertical blank period VB.

Claim 2 (original): The method as claimed in claim 1, after the step (c), start vertical signals STV are generated after at least a third cycle C3 during the vertical blank period VB.

Claim 6 (currently amended): A method of processing signals of a timing controller of a liquid crystal display module, comprising the steps of:

- (a) receiving a data enable signal DE which has a vertical blank period;
- (b) decoding the signal to generate a vertical synchronizing signal;
- (c) generating a gate clock signal CPV which has a plurality of gate clock cycles C1-Cn;
- (d) after a rising edge or a falling edge of the vertical synchronizing signal, generating a plurality of gate-on enable signals OE simultaneously according to the plurality of gate clock cycles C1-Cn of the gate clock signal CPV;
- (e) after a rising edge or a falling edge of the vertical synchronizing signal, generating start vertical signals STV before the end of the vertical blank period VB and after at least a gate clock cycle C1 during the vertical blank period VB, wherein the start vertical signals STV includes a first start vertical signal STV1 to determine a start scan location of a frame and a second start vertical signal STV2 to offset flicker and display brightness of the liquid crystal display; and
- (f) pausing output of CPV, STV₁, and OE until the end of the vertical blank period VB.

Claim 7 (previously presented): The method as claimed in claim 6, wherein in step (c), start vertical signals STV are generated after at least a third cycle C3 during the vertical blank period VB.

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